FIG.1

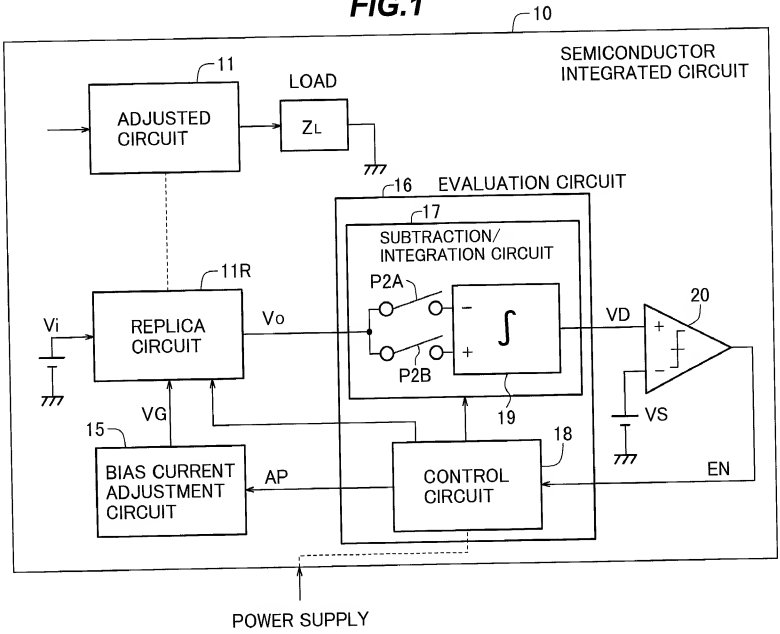
10
SEMICONDUCTOR INTEGRATED CIRCUIT
11
ADJUSTED CIRCUIT
LOAD
ZL
16
EVALUATION CIRCUIT
17
SUBTRACTION/ INTEGRATION CIRCUIT
P2A
P2B
11R
REPLICA CIRCUIT
Vi
Vo
VD
20
VS
VG
15
BIAS CURRENT ADJUSTMENT CIRCUIT
AP
CONTROL CIRCUIT
18
19
EN
POWER SUPPLY

FIG.2

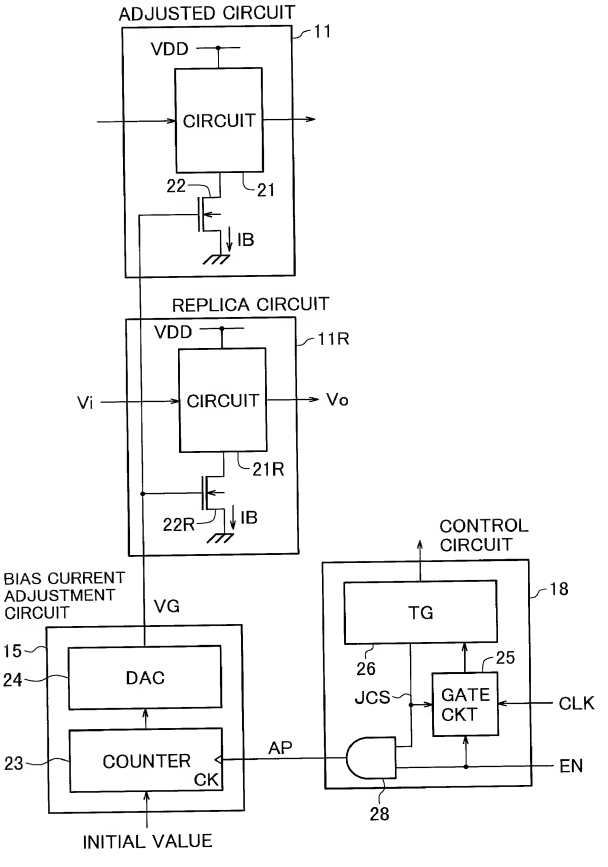
ADJUSTED CIRCUIT
11
VDD
CIRCUIT
22
21
IB
REPLICA CIRCUIT
VDD
11R
Vi
CIRCUIT
Vo
21R
22R
IB
CONTROL CIRCUIT
18
TG
26
25
JCS
GATE CKT
CLK
EN
28
BIAS CURRENT ADJUSTMENT CIRCUIT
VG
15
24
DAC
23
COUNTER
CK
AP
INITIAL VALUE

FIG.3

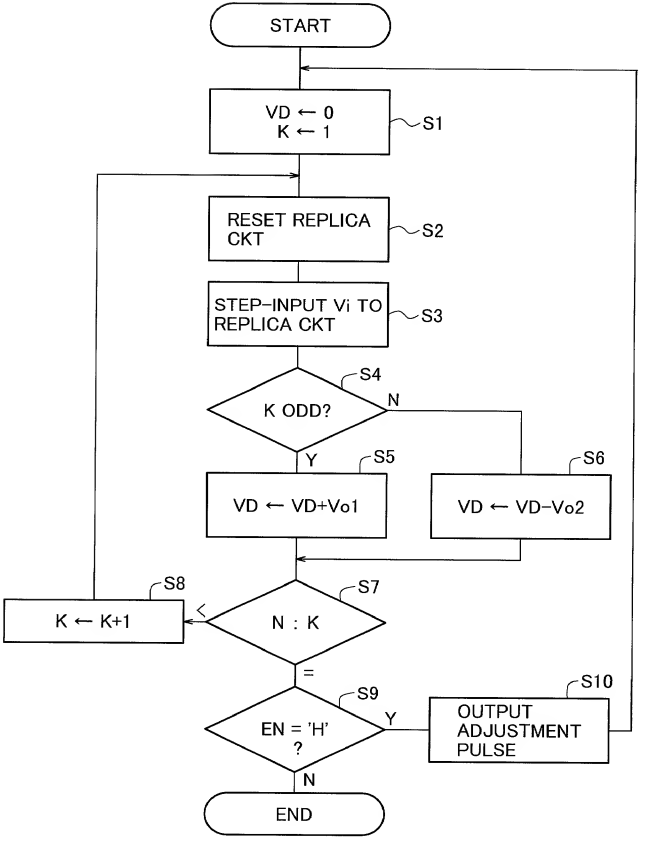
START
VD ← 0
K ← 1
S1
RESET REPLICA CKT
S2
STEP-INPUT Vi TO REPLICA CKT
S3
K ODD?
S4
N
Y
VD ← VD+Vo1
S5
VD ← VD-Vo2
S6
N : K
S7
<
=
K ← K+1
S8
EN = 'H' ?
S9
Y
N
OUTPUT ADJUSTMENT PULSE
S10
END

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FIG.4(A)

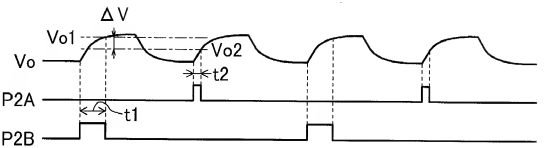

FIG.4(B)

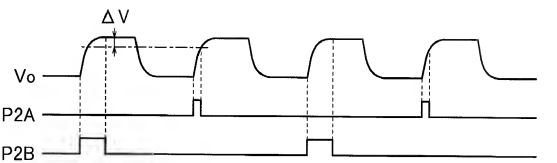

FIG.4(C)

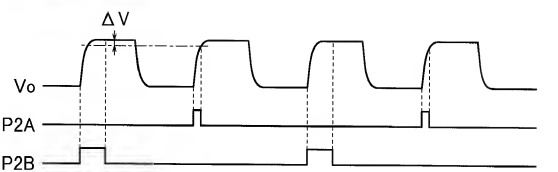

FIG.5(A)

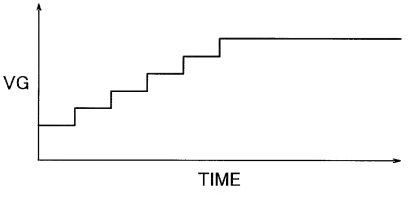

FIG.5(B)

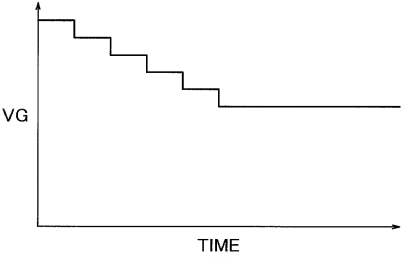

FIG.5(C)

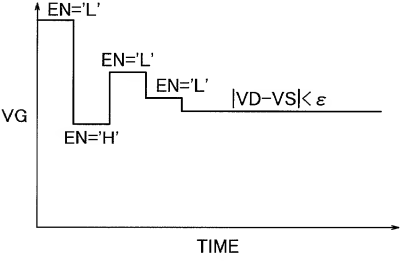

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FIG.6

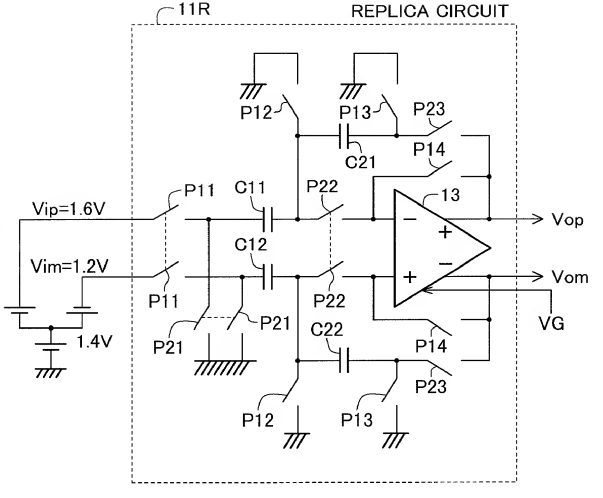

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FIG.7

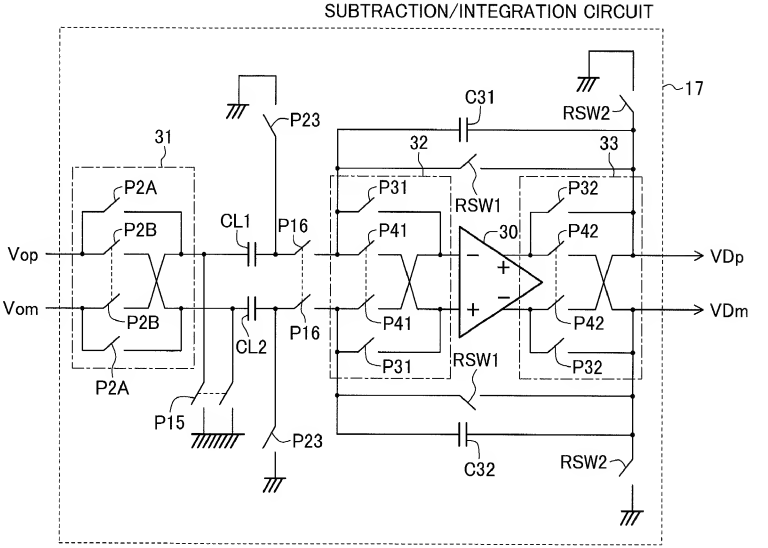

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FIG.8

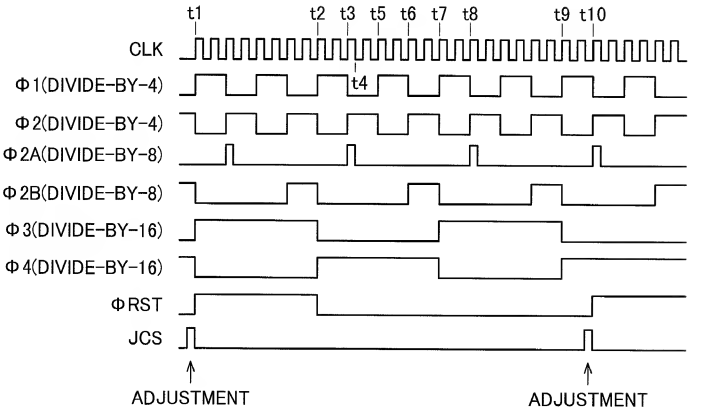

FIG.9
prior art

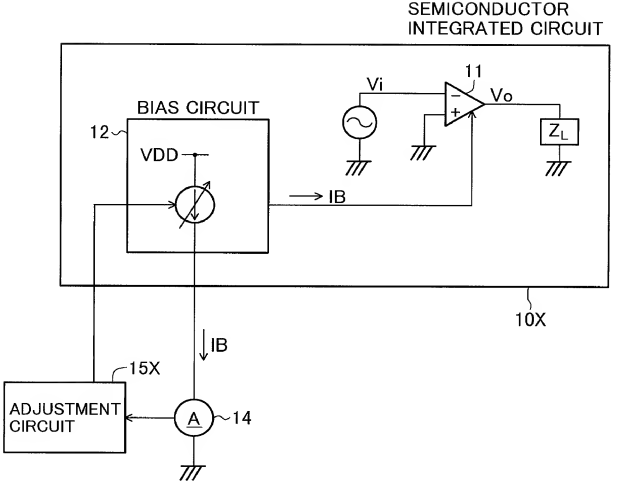

FIG.10
prior art

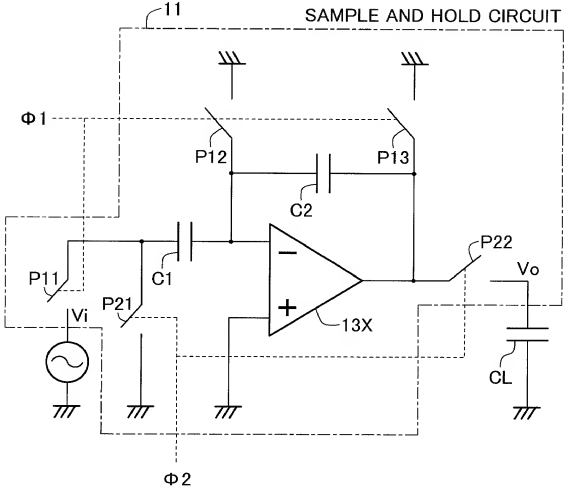

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FIG.11
prior art

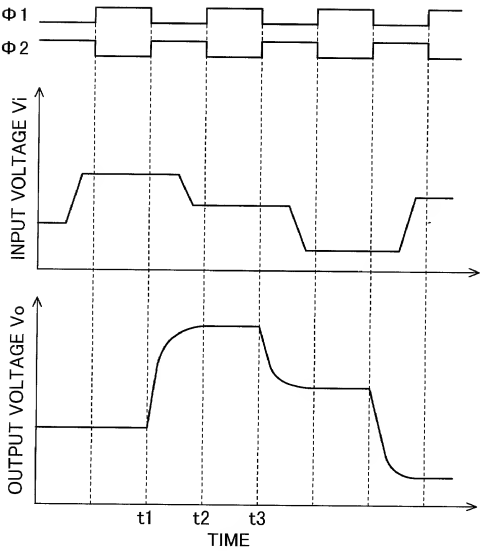
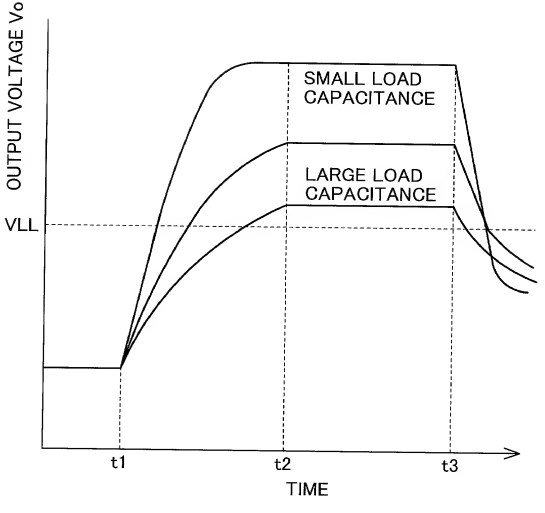
FIG.12
prior art